WHAT IS CLAIMED IS:

1. An array substrate for a transflective liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line, the gate line and the data line defining a pixel region having a transmissive portion and a reflective portion;

a gate electrode connected to the gate line;

source and drain electrode spaced apart from each other over the gate electrode, the source electrode being connected to the data line;

a reflective layer at the same layer as the source and drain electrodes, the reflective layer being disposed in the pixel region and having a transmissive hole corresponding to the transmissive portion; and

a pixel electrode connected to the drain electrode, the pixel electrode being disposed in the pixel region,

wherein the source and drain electrodes and the reflective layer have multiple layers of metal,

wherein a top layer of the multiple layers includes a reflective metallic material.

2. The array substrate according to claim 1, wherein the reflective metallic material is a metal including aluminum (Al).

3. The array substrate according to claim 2, wherein the metal is aluminum-neodymium (AlNd).

4. The array substrate according to claim 1, wherein the data line and the reflective layer are spaced apart from each other by a distance of about 5 μm to about 7 μm.

5. The array substrate according to claim 1, further comprising first to third insulating layers and a semiconductor layer, wherein the first insulating layer is formed on the gate electrode and the gate line, wherein the semiconductor layer is formed on the first insulating layer, wherein the second and third insulating layers are sequentially formed on the source and drain electrodes and the reflective layer, and wherein the second and third insulating layers have a drain contact hole exposing the drain electrode.

6. The array substrate according to claim 5, further comprising first and second capacitor electrodes, wherein the first capacitor electrode has the same layer as the gate line, wherein the second capacitor electrode has the same layer as the data line, wherein the second capacitor electrode overlaps the first capacitor electrode.

7. The array substrate according to claim 6, wherein the first insulating layer is interposed between the first and second capacitor electrodes, wherein the second capacitor electrode is connected to the pixel electrode through a capacitor contact hole in the second and third insulating layers.

8. A method of fabricating an array substrate for a transflective liquid crystal display device, comprising:

forming a gate electrode and a gate line on a substrate through a first mask process;

forming a first insulating layer on the gate electrode and the gate line;

forming a semiconductor layer on the first insulating layer over the gate electrode through a second mask process;

forming source and drain electrodes on the semiconductor layer, a data line crossing the gate line, and a reflective layer on the first insulating layer through a third mask process, the source and drain electrodes being spaced apart from each other, the source electrode being connected to the data line, the gate line and the data line defining a pixel region having a transmissive portion and a reflective portion, the reflective layer being disposed in the pixel region and having a transmissive hole corresponding to the transmissive portion, the source and drain electrodes, the data line and the reflective layer having multiple layers of metal, a top layer of the multiple layers including a reflective metallic material;

forming second insulating layer on the source and drain electrodes, the data line and the reflective layer through a fourth mask process, the second insulating layer having a drain contact hole exposing the drain electrode; and

forming a pixel electrode on the third insulating layer through a fifth mask process, the pixel electrode including a transparent conductive material, the pixel electrode being connected to the drain electrode through the drain contact hole.

9. The method according to claim 1, further comprising:

forming a first align key in a non-display region of the substrate through the third mask process; and

forming the second insulating layer on the first align key through the fourth mask process, the second insulating layer having an open portion exposing the first align key.

10. The method according to claim 9, further comprising forming a second align key on the substrate through the first mask process, wherein the second align key corresponds to the first align key.

11. The method according to claim 8, wherein the data line and the reflective layer are spaced apart from each other by a distance of about 5 μm to about 7 μm.

12. The method according to claim 8, further comprising forming first and second capacitor electrodes, wherein the first capacitor electrode is formed on the substrate through the first mask process, wherein the second capacitor electrode is formed on the first insulating layer through the third mask process and overlaps the first capacitor electrode.

13. The method according to claim 12, further comprising forming a capacitor contact hole in the second insulating layer through the fourth mask process, wherein the capacitor contact hole exposes the second capacitor electrode, the pixel electrode is connected to the second capacitor electrode through the capacitor contact hole.

14. A method of fabricating an array substrate for a transflective liquid crystal display device, comprising:

forming a gate electrode and a gate line on a substrate;

forming a first insulating layer on the gate electrode and the gate line;

forming a semiconductor layer on the first insulating layer, the semiconductor layer having an active layer and an ohmic contact layer;

forming source and drain electrodes, a data line and a reflective layer having multiple layers on the first insulating layer at the same time, wherein the gate line and the data line define a pixel region having a transmissive portion and a reflective portion; and

forming a pixel electrode of a transparent conductive material electrically connected to the drain electrode.

15. The method according to claim 14, further comprising forming an first align key at the same time as the source and drain electrodes, the data line and the reflective layer on the first insulating layer.

16. The method according to claim 15, further comprising forming a second align key at the same time as the gate electrode and the gate line, wherein the second align key corresponds to the first align key.

17. The method according to claim 14, further comprising:

forming second insulating layer on the source and drain electrodes, the data line and the reflective layer, the second insulating layer having a drain contact hole exposing the drain electrode.

18. The method according to claim 17, wherein the pixel electrode is electrically connected to the drain electrode through the drain contact hole.

19. The method according to claim 14, wherein the data line and the reflective layer are spaced apart such that the data line and the reflective layer are electrically insulated.

20. The method according to claim 14, wherein the top layer of the reflective layer is of high reflectance and the bottom layer of the reflective layer is of high chemical corrosion resistance.